Ultra-High-Speed GaAs Monolithic Prescaler and Phase Frequency Comparator IC

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Abstract—**A high-speed, low-power prescaler and phase frequency comparator (PFC) IC for a phase-lock stable oscillator was designed and fabricated on a single chip using GaAs MESFET BFL circuitry. The gate width of the master-slave *T*-type flip-flops used in designing the 1/32 frequency divider prescaler was determined by circuit simulations. The fabricated 1/32 prescaler operated up to 8.0 GHz while the fabricated monolithic prescaler and PFC IC performed stable division, and phase and frequency comparison at input frequencies up to 4.8 GHz with a chip power dissipation of only 715 mW.**

I. Introduction

BECAUSE OF THE recent progress in the complexity and performance of GaAs high-speed logic IC's, their applications in various fields are increasing [1]. Their application, in particular, to local oscillator circuits in satellite [2] and microwave communication systems has been made due to their characteristics of high-speed operation, low-power consumption, and resistance to radiation. The schematic diagram of a stabilized local oscillator system is shown in Fig. 1. The design of a stabilized voltage-controlled oscillator (VCO), requires a prescaler and a PFC. The prescaler divides the VCO output frequency and the PFC outputs a VCO control signal for comparing the divided frequency of the VCO to the output frequency of a stable oscillator such as a crystal oscillator. A conventional 1/32 frequency divider prescaler using GaAs MESFET's can operate up to 6 GHz [3]. A conventional PFC using GaAs MESFET's can operate up to 600 MHz at 60 mW [4]. To simplify the construction of a phase-lock loop, to improve phase and frequency stability, and to reduce power consumption, a monolithic prescaler and PFC IC operating at higher frequency with less power is needed.

The first attempt to fabricate a GaAs monolithic ultra-high-speed and low-power prescaler and a PFC IC is described in this paper. As for a basic gate, GaAs BFL [5], [6] using only normally-on FET's is advantageous from the viewpoints of high-speed operation, large operation margin, strong performance against large fan-out, and easy fabrication. Here, the basic gate adopted is a BFL circuit with a source follower needed for high-speed operation [7]. Circuit simulations of the prescaler and PFC operation were performed for determining FET gate widths used in constructing the circuit. The fabrication process uses the closely spaced electrode structure [8]. The monolithic prescaler and PFC IC performed stable division, and phase and frequency comparison up to 4.8 GHz input frequency at only 715 mW, and the prescaler section operated up to 8.0 GHz. The fabrication yield for a 1/32 prescaler section operating at more than 5.3 GHz in the laboratory was as much as 21/26 on one wafer.

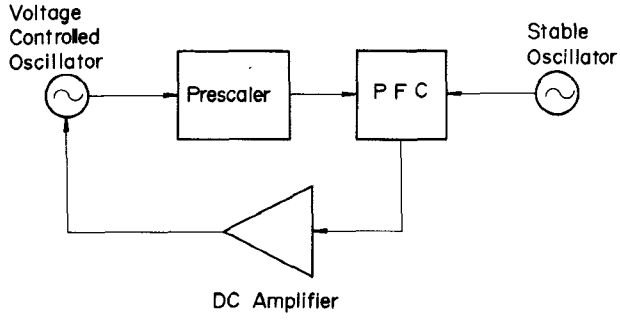

Fig. 1. Schematic diagram of a stabilized local oscillator system.

II. Circuit Design

A circuit diagram of a master-slave *T*-type flip-flop is shown in Fig. 2 [5]. The typical bias conditions were $V_{DD} = 3.5$ V and $V_{SS} = -2$ V. For the basic gate mentioned above, a BFL circuit is used with a source follower which gives large driving capability and high-speed operation. In the circuit, the gate widths of FET's and diodes are equal to W_g. The FET threshold voltage of -0.8 V and two-level shift diodes were adopted in order to obtain high-speed operation and low-power consumption [7]. A gate length of 0.7 μm is used for good fabrication yield in the present process. The circuit was designed using FET and diode models including parasitic capacitances [9]. These were fitted to FET and diode characteristics fabricated by the process described later. The circuit simulations were performed using SPICE II.

The simulated result of the relationship between the FET gate width of a master-slave *T*-type flip-flop and the

Manuscript received October 28, 1985; revised February 4, 1986.

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IEEE Log Number 8608333.

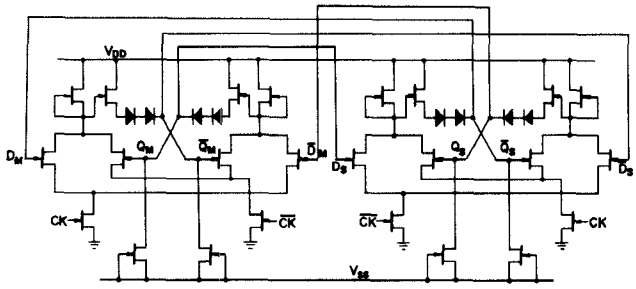

Fig. 2. Circuit schematic diagram of a master-slave T-type flip-flop.

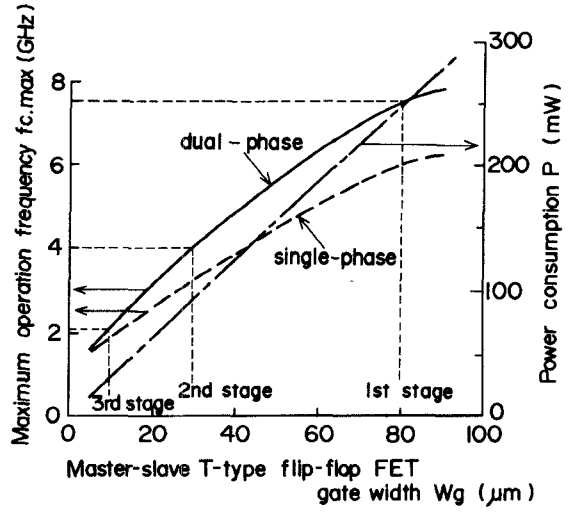

Fig. 3. Simulated relationship between the FET gate width of a master-slave T-type flip-flop and the maximum operation frequency and power consumption.

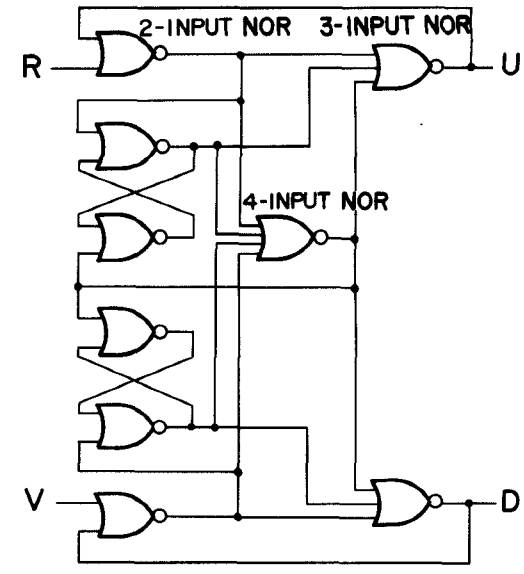

Fig. 4. Logic diagram of a phase-frequency comparator.

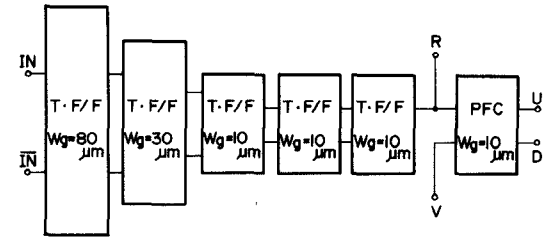

Fig. 5. Block diagram of a monolithic 1/32 prescaler and PFC IC.

maximum operation frequency and the power consumption is shown in Fig. 3. The solid line indicates the dual-phase input sensitivity, and the broken line the single-phase input sensitivity. For the dual-phase input case, if the 1/32 prescaler first stage 1/2 frequency divider uses an 80-μm gate width, the maximum operation frequency is 7.5 GHz, and the input frequency of the second stage 1/2 frequency divider becomes 3.75 GHz. Thus, the FET gate width of the second stage can be 30 μm in order to achieve low-power consumption in prescaler operation. In the same way, the FET gate width of the third stage can be 10 μm. The FET gate widths for the fourth and fifth stages were chosen to be 10 μm because of unstable operation below the 10-μm gate width. In the single-phase case, the maximum operation frequency was lower than that in the dual-phase case (e.g., by 1.5 GHz with an 80-μm gate width).

A logic diagram of a PFC is shown in Fig. 4. The PFC is constructed with 9 NOR gates. As with the prescaler, a BFL circuit with a source follower is used as a basic gate with a FET threshold voltage of -0.8 V. The gate widths of the FET's and diodes are chosen to be equal to $W_g = 10$ μm in order to obtain low-power consumption [4].

The block diagram of a monolithic 1/32 prescaler and PFC IC described above is shown in Fig. 5. The total NOR gate number of a 1/32 prescaler and PFC is 29.

III. IC Fabrication

A 2-in diameter GaAs wafer is used. The fabrication process used a closely spaced electrode structure [8]. An active layer was formed by ion implantation.

The FET gate length is 0.7 μm, FET average threshold voltage $\bar{V}_t$ is -0.80 V measured across a 2-in diameter wafer, and its standard deviation is 101 mV. The average transconductance $\bar{g}_m$ is 137 mS/mm($V_{GS} = 0$ V, $V_{DS} = 2$ V), its standard deviation is 8.5 mS/mm, and the average drain conductance is 14 mS/mm.

The chip size of the monolithic prescaler and PFC IC is 2.65×1.1 mm^2. Test cells on the same mask included a 1/2 static frequency divider of gate width 40 μm, and 17-stage ring oscillators of gate widths 80 and 20 μm. These circuit geometries were optimized and made compact by symmetric circuit arrangements and short interconnections.

IV. Performance

A. Frequency Divider and PFC

Propagation delay times of fabricated 17-stage ring oscillators of gate widths 80 and 20 μm were 43 ps/gate at 44 mW/gate and 56 ps/gate at 12 mW/gate, respectively. These results correspond to simulation results calculated from the above circuit simulation models regarding pattern effects.

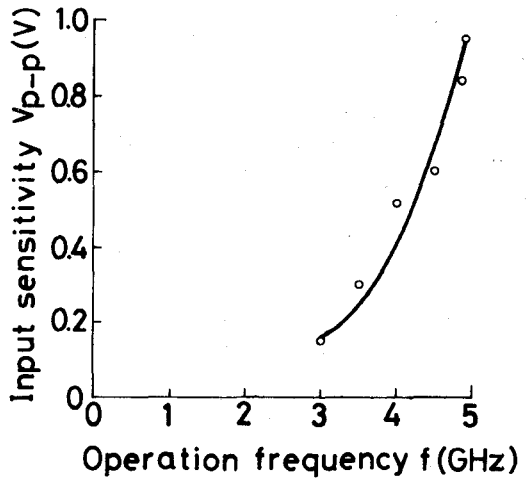

Fig. 6. Input sensitivity V_{p-p} against frequency of a fabricated 1/2 frequency divider with a 40 μm gate width.

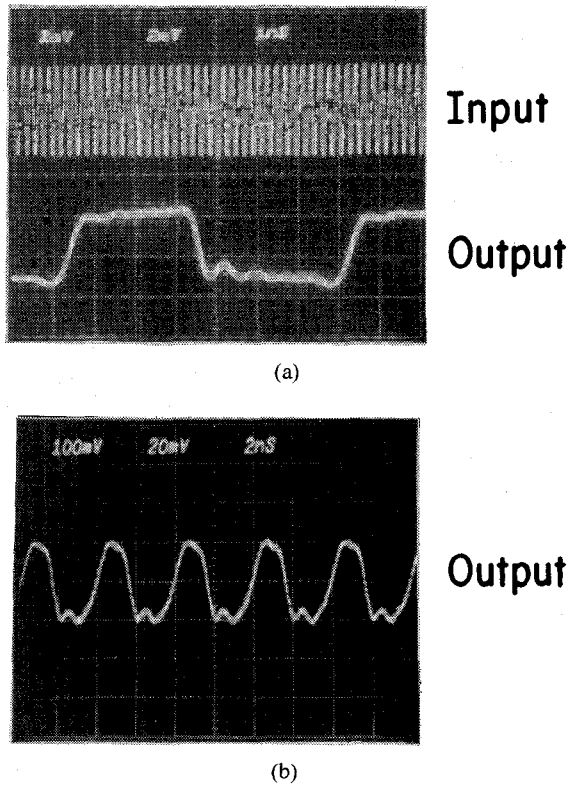

Fig. 7. Operation waveforms of the 1/32 prescaler section. (a) Waveforms at 4.8 GHz. Upper trace: Input; Lower trade: Output signal (into 50 Ω). (b) Output waveform at 8.0 GHz (40dB att.).

Fig. 6 shows the input sensitivity V_{p-p} against operation frequency of the fabricated 1/2 frequency divider with a 40-μm gate width. This figure shows the dual-phase input sensitivity. Here, the maximum operation frequency is 4.8 GHz at 84 mW. This result almost corresponds to the simulation result in Fig. 3.

We investigated the characteristics of the 1/32 prescaler section of a monolithic IC. Fig. 7(a) shows input and output waveforms of the 1/32 prescaler at 4.8-GHz single-phase input frequency, and Fig. 7(b) shows the output waveform at 8.0-GHz dual-phase input frequency.

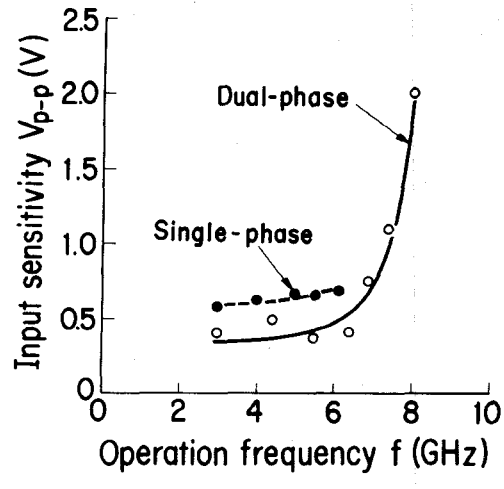

Fig. 8. Input sensitivity V_{p-p} against operation frequency of the fabricated 1/32 prescaler section.

Fig. 8 shows the input sensitivity V_{p-p} against operation frequency of the 1/32 prescaler. The solid line indicates the dual-phase input sensitivity and the broken line indicates the single-phase input sensitivity where the other input is set at the proper reference voltage. Maximum operation frequencies in dual-phase and single-phase cases are 8.0 and 6.0 GHz, respectively. Below an input frequency of 5.0 GHz, the bias condition is fixed around $V_{DD} = 3.5$ V and $V_{SS} = -2.0$ V, but above an input frequency of 5.0 GHz, the bias condition must be adjusted according to the input frequency.

We investigated characteristics of the PFC section of the monolithic IC, using R and V inputs as shown in Fig. 5. Fig. 9(a) shows the dc phase comparison performance of the fabricated PFC. The operation frequency is 250 MHz. The output dc voltage varied periodically every 2π owing to the difference between the two input signal phases. Fig. 9(b) shows the dc frequency comparison performance. The output dc voltage jumps from the low level to the high level abruptly around 300 MHz, which was the one fixed input frequency. These results indicate that the fabricated PFC performed stable phase and frequency comparison. Stable frequency comparison was observable up to 450 MHz with the fabricated PFC.

B. Total Characteristics

Fig. 10 shows a system for measurement of the overall characteristics. In this measurement, the prescaler is operated by a single-phase input. The PFC V input frequency is fixed at 144 MHz (4.62 GHz/32), the prescaler input frequency is varied from 4.5 to 4.8 GHz, and the dc voltage between PFC outputs of U and D is measured. The prescaler input voltage is 1.6 V_{p-p}. Fig. 11 shows a typical performance. The output dc voltage jumps from the high level to the low level abruptly around the prescaler input frequency of 4.62 GHz. These results indicate that the monolithic prescaler and PFC IC performed stable 1/32 division and frequency comparison operation up to 4.8 GHz. Total power consumption is only 715 mW. The reason that the monolithic prescaler and PFC IC operates

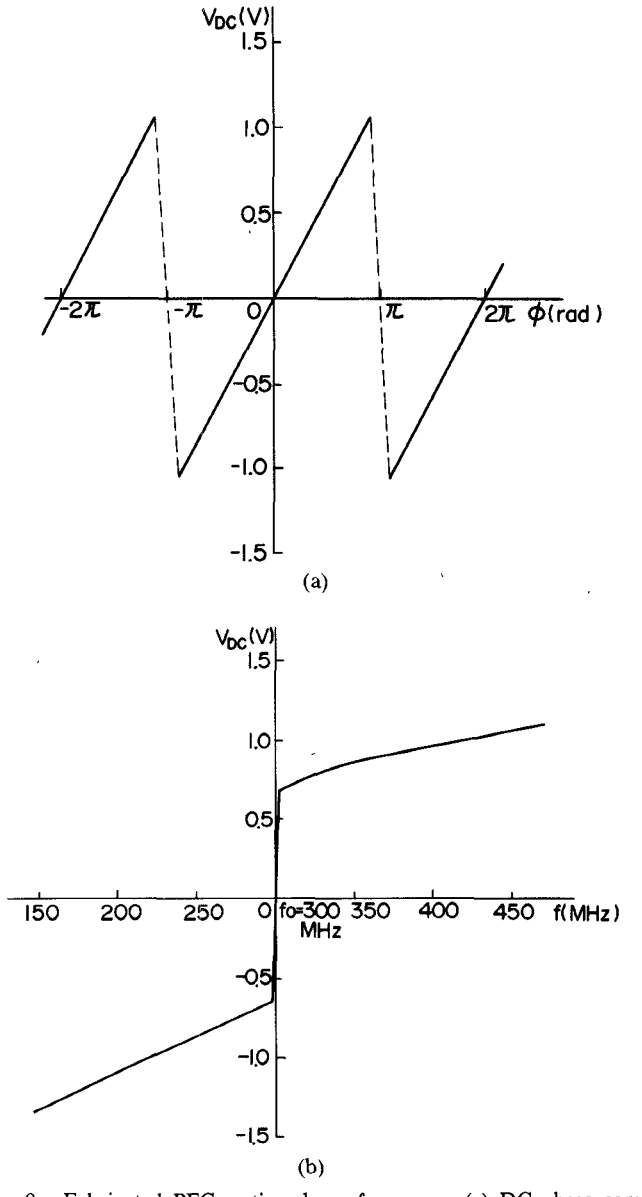

Fig. 9. Fabricated PFC section dc performances. (a) DC phase comparison performance ($f = 250$ MHz). (b) DC frequency comparison performance.

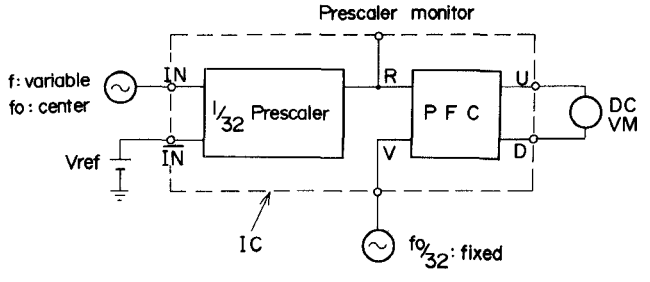

Fig. 10. System for measurement of overall characteristics.

only to 4.8 GHz is the difference between the optimum bias condition of the prescaler and the PFC. The fabrication yield in the laboratory with 1/32 prescalers operating at more than 5.3 GHz by dual-phase inputs is as much as 21/26. The fabrication yield for the PFC section is almost 100 percent.

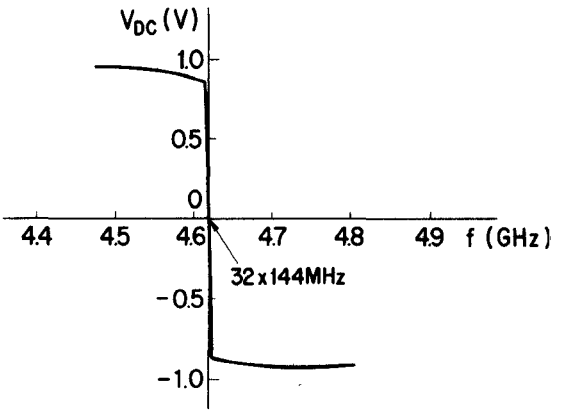

Fig. 11. Overall characteristics of the device.

V. Conclusion

The monolithic prescaler and PFC IC is used to stabilize local oscillator circuits in satellite and microwave communication systems. It has been designed and fabricated for the first time using GaAs MESFET BFL circuits, which enables high-speed operation and large operation margin. The FET gate widths for the master-slave T-type flip-flops used in constructing a 1/32 prescaler and the PFC were optimized for the prescaler and PFC IC to enable high-speed operation and low-power consumption. The fabricated 1/32 prescaler operates up to 8.0 GHz and the fabricated monolithic prescaler and PFC IC performed stable division, and phase and frequency comparison up to 4.8-GHz prescaler input frequency with a power dissipation of only 715 mW. The fabrication yield for the 1/32 prescaler section operating at more than 5.3 GHz in the laboratory was as much as 21/26 on one wafer.

As described above, this monolithic prescaler and PFC IC using a GaAs BFL circuit can be used effectively in satellite and microwave communication applications.

Acknowledgment

The authors wish to acknowledge M. Hirayama, M. Idda, and Dr. T. Takada for their helpful discussions and suggestions. They also wish to thank Dr. T. Sugeta, Dr. M. Ohmori, Dr. T. Ikegami, and Dr. M. Fujimoto for their continuous encouragement.

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